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10/808,389	03/25/2004	Satoru Konishi	501.43628X00	5559

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EXAMINER	
KUNZER, BRIAN	
ART UNIT	**PAPER NUMBER**
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,389	KONISHI ET AL.	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2, and 4-13* is/are rejected.

7)☒ Claim(s) *1-3,8,10, and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on March 26, 2003. It is noted, however, that applicant has not filed a certified copy of the 2003-086158 application as required by 35 U.S.C. 119(b).

Claim Objections

1. Claims 1, 2, 8, 10, and 12 are objected to because of the following informalities:

the claims recite a first frequency and a second frequency (including a third and fourth frequency for claim 2), but does not claim that these two frequencies are distinct from one another nor do these claims claim that the first and second circuits of either chip are independent of each other. Therefore any stacked array of two or more chips would be able to read on the claims as prior art since a single chip contains millions of circuits and operates at a single frequency. Applicant would be advised to amend claims 1, 2, 8, 10, and 12 on these grounds.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 12 and 13 (dependent on claim 12) are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 12 recites the limitation "the wires bonded to the second circuits of the second semiconductor chip" and "the wires bonded to the first circuits of the second semiconductor chip". There is no previous mention of the wires bonded to the second semiconductor chip. There is insufficient antecedent basis for this limitation in the claim.

5. Furthermore, claim 12 recites the limitation of two wires to "face each other". This has an indefinite meaning as a wire is usually viewed as a one-dimensional object whereas the term "face" is used to describe at least a two-dimensional object or if the wire is considered as a three-dimensional object, it is unclear which parts of the wires are facing each other.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 4, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamikuri (US Patent No. 6,563,206) in view of Winslow (US Patent No. 6,803,817).

8. With respect to claim 1, Kamikuri teaches, from fig. 2, a semiconductor device comprising:

a printed wiring board (37) having a top surface, and a backside surface, on the side of the printed wiring board, opposite from the top surface;

a second semiconductor chip (33) mounted over the top surface of the printed wiring board (37);

a first semiconductor chip (51) disposed so as to overlie the second semiconductor chip (33);

a plurality of conductive wires (45) electrically bonding the first semiconductor chip (51) to the printed wiring board (37);

9. However, Kamikuri does not explicitly teach that there are more than two circuits on the chip or that there is a first and second frequency at which the circuits operate.

10. Winslow, drawn to dual band power amplifiers, teaches, from fig. 2, a semiconductor device with a single chip including first circuits (14b) operated at a first frequency and second circuits (14a) operated at a second frequency. (see column 3, lines 48-51)

11. Therefore it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the stacked arrangement of Kamikuri with the device of Winslow - a double stack of dual band amplifiers wherein the first circuit of the first semiconductor chip is disposed opposite to the second circuits of the second semiconductor chip, while the second circuit of the first semiconductor chip is disposed opposite to the first circuits of the second semiconductor chip - because the arrangement would reduce the area covered by the power amplifier chip on the printed wiring board, thus consuming less space, making further miniaturization of devices (such as cell phones) possible. (See column 1, lines 22-26 in 6,563,206 and column 1, lines 15-18 in 6,803,817)

12. With respect to claim 4, Winslow teaches the first and second frequencies are in the ranges of 880 ~ 915 MHz and 1710 ~1785 MHz., respectively. (see column 1, lines 27-31)

13. With respect to claim 6, Kamikuri teaches, from fig. 2, wherein the second semiconductor chip (33) is bonded to the printed wiring board (37) by flip bonding.

14. With respect to claim 7, Kamikuri combined with Winslow teach, from fig. 2, the said semiconductor device, wherein a first wire (45 on left side of fig.2) that is electrically bonded to the first circuit (left side of chip 51) of the first semiconductor chip (51) is disposed opposite to a first wiring of the printed wiring board (49 on left side), which is electrically bonded to the second circuits (left side of chip 33) of the second semiconductor chip (33), respectively, while a second wire (45 on right side of fig.2) that is electrically bonded to the second circuit (right side of chip 51) of the first semiconductor chip (51) is disposed opposite to a second wiring (49 on right side) of the printed wiring board (37), which is electrically bonded to the first circuits (right side of chip 33) of the second semiconductor chip (33), respectively. (see fig. 3)

15. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamikuri (US Patent No. 6,563,206) and Winslow (US Patent No. 6,803,817) as applied to claim 1 above, and further in view of Hashemi (US Patent No. 6,674,337).

16. Kamikuri in combination with Winslow teach the semiconductor device of claim 1.

17. However, Kamikuri in combination with Winslow do not teach the semiconductor device operating at more than two frequencies in each chip.

18. Hashemi, drawn to multi-band amplifiers, teaches an amplifier circuit allowing two or more frequency bands to be used. (see column 3, lines 33-37)

19. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to use the device arrangement of Kamikuri and Winslow in conjunction with the circuits of Hashemi, because this simply allows amplification of more frequency bands, thus providing reception for more telecommunication systems, for example. (see column 1, lines 45-57 of 6,674,337

20. Claims 1, 5, and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo (US Patent No. 6,414,384) in view of Winslow (US Patent No. 6,803,817).

21. With respect to claim 1, Lo teaches, from fig. 4, a semiconductor device comprising:

a printed wiring board (402) having a top surface, and a backside surface, on the side of the printed wiring board, opposite from the top surface;

a second semiconductor chip (406) mounted over the top surface of the printed wiring board (37);

a first semiconductor chip (408) disposed so as to overlie the second semiconductor chip (406);

a plurality of conductive wires (410b) electrically bonding the first semiconductor chip (408) to the printed wiring board (402);

22. However, Kamikuri does not explicitly teach that there are more than two circuits on the chip or that there is a first and second frequency at which the circuits operate.

23. Winslow, drawn to dual band power amplifiers, teaches, from fig. 2, a semiconductor device with a single chip including first circuits (14b) operated at a first frequency and second circuits (14a) operated at a second frequency. (see column 3, lines 48-51)

24. Therefore it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the stacked arrangement of Kamikuri with the device of Winslow - a double stack of dual band amplifiers wherein the first circuit of the first semiconductor chip is disposed opposite to the second circuits of the second semiconductor chip, while the second circuit of the first semiconductor chip is disposed opposite to the first circuits of the second semiconductor chip - because the arrangement would reduce the area covered by the power amplifier chip on the printed wiring board, thus consuming less space, making further miniaturization of devices (such as cell phones) possible. (See column 1, lines 22-26 in 6,414,384 and column 1, lines 15-18 in 6,803,817)

25. With respect to claim 5, Kamikuri teaches, from fig. 2, the said semiconductor device wherein the second semiconductor chip (406) is electrically bonded to the printed wiring board (402) with conductive wires (410a).

26. With respect to claim 8, Lo teaches, from fig. 4A, a semiconductor device comprising:

a printed wiring board (402) having a top surface, and a backside surface, on the side of the printed wiring board, opposite from the top surface;

a second semiconductor chip (406) mounted over the top surface of the printed wiring board (402);

a first semiconductor chip (408) disposed so as to overlie the second semiconductor chip (406);

a plurality of wires (410a and 410b) electrically bonding the first semiconductor chip (408) and the second semiconductor chip (406) to the printed wiring board, respectively.

27. However, Lo does not explicitly teach that there are more than two circuits on the chip or that there is a first and second frequency at which the circuits operate.

28. Winslow, drawn to dual band power amplifiers, teaches, from fig. 2, a semiconductor device with a single chip including first circuits (14b) operated at a first frequency and second circuits (14a) operated at a second frequency. (see column 3, lines 48-51)

29. Therefore it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the stacked arrangement of Kamikuri with the device of Winslow – a double stack of dual band amplifiers wherein the first circuit of the first semiconductor chip is disposed opposite to the second circuits of the second semiconductor chip, while the second circuit of the first semiconductor chip is disposed opposite to the first circuits of the second semiconductor chip (see fig. 4A for arrangement of wires, electrodes, and chips)- because the arrangement would reduce the area covered by the power amplifier chip on the printed wiring board, thus consuming less space, making further miniaturization of devices (such as cell phones) possible. (See column 1, lines 22-26 in 6,414,384 and column 1, lines 15-18 in 6,803,817)

30. With respect to claim 9, Lo combined with Winslow teaches, from fig. 4A the said semiconductor device, wherein the wiring direction of the plurality of wires (410b) bonded to the plurality of first electrodes (422 on left side of fig.4A) and second electrodes (422 on right side

of fig.4A) of the first semiconductor chip (408), respectively, intersects the wiring direction of the plurality of wires bonded to the plurality of first electrodes (422 on left side of fig.4B) and second electrodes (422 on right side of fig.4B) of the second semiconductor chip (406), respectively, at right angles. (see fig. 4B)

31. With respect to claim 10, Lo teaches, from fig. 4, a semiconductor device comprising:

a printed wiring board (402) having a top surface, and a backside surface, on the side of the printed wiring board, opposite from the top surface;

a second semiconductor chip (406) mounted over the top surface of the printed wiring board (402);

a first semiconductor chip (408) disposed so as to overlie the second semiconductor chip (406);

a plurality of conductive wires (410b) electrically bonding the first semiconductor chip (408) to the printed wiring board (402);

32. However, Lo does not explicitly teach that there are more than two circuits on the chip or that there is a first and second frequency at which the circuits operate or that a wiring layer for GND (ground) is provided between the first and second circuits.

33. Winslow, drawn to dual band power amplifiers, teaches, from fig. 2, a semiconductor device with a single chip including first circuits (14b) operated at a first frequency and second circuits (14a) operated at a second frequency (see column 3, lines 48-51). Winslow also teaches that there is a wiring layer (24''') for ground (22) between the first circuits (14b) and second circuits (14a). (See fig. 5 and column 5, lines 25-39)

34. Therefore it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the stacked arrangement of Lo with the device of Winslow - wherein a first wiring layer for GND is provided between the first circuit and the second circuit of the first semiconductor chip, and a second wiring layer for GND is provided between the first circuits and the second circuits of the second semiconductor chip - because the arrangement would; one, reduce the area covered by the power amplifier chip on the printed wiring board, thus consuming less space, making further miniaturization of devices (such as cell phones) possible (See column 1, lines 22-26 in 6,414,384 and column 1, lines 15-18 in 6,803,817); and two, reduce the interference between the circuits causing undesirable noise. (see column 3, lines 3-5 in 6,803,817)

35. With respect to claim 11, Lo combined with Winslow teach the semiconductor device according to claim 10, wherein the first circuit (left hand side of 408) of the first semiconductor chip (408) is disposed opposite to the second circuits (right hand side of 406) of the second semiconductor chip (406), and the second circuit (right hand side of 408) of the first semiconductor chip (408) is disposed opposite to the first circuits (left hand side of 406) of the second semiconductor chip (406). (See fig. 4B of Lo)

36. With respect to claim 12, Lo teaches, from fig. 4A, a semiconductor device comprising:

a printed wiring board (402) having a top surface, and a backside surface, on the side of the printed wiring board, opposite from the top surface;

a second semiconductor chip (406) mounted over the top surface of the printed wiring board (402);

a first semiconductor chip (408) disposed so as to overlie the second semiconductor chip (406);

a plurality of wires (410a and 410b) electrically bonding the first semiconductor chip (408) and the second semiconductor chip (406) to the printed wiring board, respectively.

37. However, Lo does not explicitly teach that there are more than two circuits on the chip or that there is a first and second frequency at which the circuits operate.

38. Winslow, drawn to dual band power amplifiers, teaches, from fig. 2, a semiconductor device with a single chip including first circuits (14b) operated at a first frequency and second circuits (14a) operated at a second frequency. (see column 3, lines 48-51)

39. Therefore it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the stacked arrangement of Kamikuri with the device of Winslow – a double stack of dual band amplifiers wherein the first circuit of the first semiconductor chip is disposed opposite to the second circuits of the second semiconductor chip, while the second circuit of the first semiconductor chip is disposed opposite to the first circuits of the second semiconductor chip (see fig. 4A for arrangement of wires, electrodes, and chips)- because the arrangement would reduce the area covered by the power amplifier chip on the printed wiring board, thus consuming less space, making further miniaturization of devices (such as cell phones) possible. (See column 1, lines 22-26 in 6,414,384 and column 1, lines 15-18 in 6,803,817)

40. With respect to claim 13, Lo combined with Winslow teach the semiconductor device according to claim 12, wherein the first circuit (left hand side of 408) of the first semiconductor chip (408) is disposed opposite to the second circuits (right hand side of 406) of the second semiconductor chip (406), and the second circuit (right hand side of 408) of the first semiconductor chip (408) is disposed opposite to the first circuits (left hand side of 406) of the second semiconductor chip (406). (See fig. 4B of Lo)

Allowable Subject Matter

41. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

42. The following is a statement of reasons for the indication of allowable subject matter: the prior record fails to show the combination of the plural stage amplifiers being staged in different chips (described in claim 3) of the stacked chip configuration described in base claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
9/8/2005

ANH D. MAI
PRIMARY EXAMINER